Final Program

1st ACM/IEEE Workshop on
Machine Learning for CAD

Monday, September 02, 2019

18:00 - 21:00	**Welcome Reception**

Tuesday, September 03, 2019

7:30 - 8:00	**Breakfast and Registration**	
8:00 - 8:15	**Introduction**	
Session 1: System-Level Optimization		
8:15 - 8:40	1.1	**Invited Talk**: Max Haeberlein, Intel. Title: **Transforming EDA with ML for the Next Generation of Designs**
8:40 - 9:00	1.2	**Machine Learning for CAD: Opportunities and Challenges** Gabor Karsai. - Vanderbilt University
9:00 - 9:20	1.3	**Combining Evolutionary Algorithms and Deep Learning for Hardware/Software Interface Optimization** Lorenzo Servadei*, Edoardo Mosca±, Jin-Hwa Lee*, Jing Yang±, Volkan Esen*, Robert Wille+ and Wolfgang Ecker*. *Infineon Technologies AG, ±Technical University of Munich, +Johannes Kepler University Linz
9:20 - 9:40	1.4	**Machine Learning Techniques to Support Many-Core Resource Management: Challenges and Opportunities** Martin Rapp*, Hussam Amrouch*, Marilyn Wolf± and Jörg Henkel* *Karlsruhe Institute of Technology, ±University of Nebraska
9:40 - 10:00	1.5	**Incremental Training and Group Convolution Pruning for Runtime DNN Performance Scaling on Heterogeneous Embedded Platforms** Lei Xun, Long Tran-Thanh, Bashir Al-Hashimi and Geoff Merrett University of Southampton
10:00 - 10:10		**Discussion and Q&A**
10:10 - 10:50		**Coffee Break**
Session 2: System-Level Modeling		
10:50 - 11:10	2.1	**Predicting Design Risk Areas** Raviv Gal, Avi Ziv, Gil Shurek and Giora Simchoni. IBM Haifa Research Lab
11:10 - 11:30	2.2	**Learning-Based Hardware/Software Performance and Power Modeling** Andreas Gerstlauer. - The University of Texas at Austin
11:30 - 11:50	2.3	**Run-Time Scenario-Based Mapping Reconfiguration Using Machine Learning Models** Jan Spieck, Stefan Wildermann and Jürgen Teich Friedrich–Alexander University Erlangen–Nürnberg
11:50 - 12:10	2.4	**Integrating Hybrid Analysis with Machine Learning Techniques for Portion Resilience Evaluation in Approximating SystemC-based Designs** Mehran Goli and Rolf Drechsler. - University of Bremen

12:10 - 12:20		**Discussion and Q&A**
12:20 - 13:30		**Lunch Break**
Session 3: Machine Learning for Physical Design		
13:30 - 13:55	3.1	**Invited Talk:** David Pan, UT Austin. Title: **Deep Learning for Agile Physical Design and Manufacturing**
13:55 - 14:15	3.2	**TransATS: Transferable Automatic Transistor Sizing with Graph Neural Networks based Reinforcement Learning** Hanrui Wang*, Kuan Wang*, Jiacheng Yang*, Linxiao Shen[+], Nan Sun[+], Hae-Seung Lee* and Song Han* *Massachusetts Institute of Technology, [+]The University of Texas at Austin
14:15 - 14:35	3.3	**Congestion-aware Global Routing using Deep Convolutional Generative Adversarial Networks** Zhonghua Zhou*, Ziran Zhu[±], Jianli Chen[±], Yuzhe Ma[+], Bei Yu[+], Tsung-Yi Ho[¥], Guy Lemieux* and Andrè Ivanov* *The University of British Columbia, [+]The Chinese University of Hong Kong, [±]Fuzhou University, [¥]National Tsing Hua University
14:35 - 14:55	3.4	**A Reinforcement Learning-Based Framework for Solving Physical Design Routing Problem in the Absence of Large Test Sets** Upma Gandhi*, Ismail Bustany[±], William Swartz[+] and Laleh Behjat* *University of Calgary, [±]Xilinx, [+]imberWolf Systems, Inc and University of Texas at Dallas
14:55 - 15:15	3.5	**Adaptive FPGA Placement Optimization via Reinforcement Learning** Kevin E. Murray and Vaughn Betz. - University of Toronto
15:15 - 15:25		**Discussion and Q&A**
15:25 - 16:00		**Coffee Break**
Session 4: Machine Learning for Memory Systems		
16:00 - 16:25	4.1	**Invited Talk:** Mark Ren, Nvidia. Title: **On the Application of Deep Learning to Design Automation: A Personal Perspective**
16:25 - 16:45	4.2	**Fast Simulation of DRAMs with Neural Networks** Johannes Feldmann*, Matthias Jung[±], Muhammad Mohsin Ghaffar* and Norbert Wehn* *Technical University of Kaiserslautern, [±]Fraunhofer
16:45 - 17:05	4.3	**Stack Usage Analysis for Efficient Wear Leveling in Non-Volatile Main Memory Systems** Christian Hakert*, Mikail Yayla*, Kuan-Hsun Chen*, Jian-Jia Chen*, Sebastian Buschjäger*, Katharina Morik*, Paul Genßler[±], Lars Bauer[±], Hussam Amrouch[±] and Jörg Henkel[±] *TU Dortmund, [±]Karlsruhe Institute of Technology
17:05 - 17:25	4.4	**Latent Factor based Error Prediction on NAND Flash Memories** Qiao Li, Yufei Cui and Chun Jason Xue. - City University of Hong Kong
17:25 - 17:40		**Discussion and Q&A**
18:00 - 19:30		**Dinner**
19:30 - 21:00		**Brain Storming Session**

Wednesday, September 04, 2019

7:30-8:15	**Breakfast**	
Session 5: Machine Learning for Design Space Exploration (DSE)		
8:15 - 8:40	5.1	**Invited Talk:** Manish Pandey, Synopsys. Title: **Enabling the Next Generation of Design Automation tools with Machine Learning**
8:40 9:00	5.2	**CAD Tool Design Space Exploration via Bayesian Optimization** Yuzhe Ma*, Ziyang Yu[+] and Bei Yu* *The Chinese University of Hong Kong, [+]The University of Hong Kong
9:00 - 9:20	5.3	**A Machine Learning Framework for Multi-Objective Design Space Exploration and Optimization of Manycore Systems** Biresh Kumar Joardar, Aryan Deshwal, Janardhan Rao Doppa and Partha Pande Washington State University
9:20 - 9:40	5.4	**FIST: A Feature-Importance Sampling and Tree-Based Method for Automatic Design Flow Parameter Tuning** Zhiyao Xie*, Guan-Qi Fang[+], Yu-Hung Huang[+], Haoxing Ren[±], Yanqing Zhang[±], Brucek Khailany[±], Shao-Yun Fang[+], Jiang Hu[¥], Yiran Chen*, Erick Carvajal Barboza[¥] and Hai Li Duke University*, National Taiwan University of Science and Technology[+], Nvidia[±], TAMU[¥]
9:40 - 10:00	5.5	**PPA Optimization Assisted with Machine-Learning-Based Design-Space Exploration** Jonathan Quijas, Ahmet Ceyhan and Will Gifford, Intel
10:00 - 10:10		**Discussion and Q&A**
10:10 - 10:50		**Coffee Break**
Session 6: Machine Learning for Power Delivery Networks (PDN)		
10:50 - 11:10	6.1	**Evolving On-Chip Power Delivery through Particle Swarm Optimization** Divya Pathak and Ioannis Savidis Drexel University
11:10 - 11:30	6.2	**PowerNet: Transferable Dynamic IR Drop Estimation via Maximum Convolutional Neural Network** Zhiyao Xie*, Haoxing Ren[+], Ye Sheng[+], Santosh Santosh[+], Brucek Khailany[+], Jiang Hu[±] and Yiran Chen* *Duke University, [+]Nvidia, [±]TAMU
11:30 - 11:50	6.3	**Machine Learning for Automated Synthesis and Refinement of Power Delivery Networks through the Design Cycle** Vidya A Chhabria*, Andrew B Kahng[+], Minsoo Kim[+], Uday Mallappa[+], Sachin S Sapatnekar* and Bangqi Xu[+] *University of Minnesota, [+]University of California San Diego
11:50 - 12:10	6.4	**Improving Robustness Against Adversarial Perturbation Attacks on DNNs for CAD** Benjamin Tan, Kang Liu, Ramesh Karri and Siddharth Garg New York University
12:10 - 12:20		**Discussion and Q&A**
12:20 - 14:00		**Lunch Break & Brain Storming**

Session 7: Machine Learning for Design Technology Co-Optimization (DTCO)		
14:00 - 14:25	7.1	**Invited Talk:** Ya-Chieh Lai, Cadence. Title: **Applications of Pattern Analysis and Machine Learning for Design for Manufacturability**
14:25 - 14:45	7.2	**Introducing Uncertainty-Enhanced Neural Network to Lithography Hotspot Detection** Yufei Cui, Qiao Li, Antoni Chan and Chun Xue City University of Hong Kong
14:45 - 15:05	7.3	**Automatic Layout Generation with Applications in Machine Learning Engine Evaluation** Haoyu Yang*, Wen Chen*, Piyush Pathak±, Frank Gennari±, Ya-Chieh Lai± and Bei Yu* *The Chinese University of Hong Kong, ±Cadence Design Systems, Inc.
15:05 - 15:25	7.4	**Predetermining CNN-Based Hotspot Detection Results Through Training Data Poisoning** Kang Liu, Benjamin Tan, Ramesh Karri and Siddharth Garg New York University
15:25 - 15:45	7.5	**Attention based Hotspot Detection** Hao Geng, Ran Chen, Haoyu Yang and Bei Yu The Chinese University of Hong Kong
15:45 - 15:55		**Discussion and Q&A**
15:55 - 16:30		**Coffee Break**
Session 8: Machine Learning for Analog Systems and Timing Analysis		
16:30 - 16:50	8.1	**An Efficient Learning Algorithm for Fast Analog Sub-circuit Identification** Jun-Jie Zhao*, Zheng-Yao Liu*, Jui-Cheng Chen* and Mark Po-Hung Lin+ *National Chung Cheng University, +National Chiao Tung University
16:50 - 17:10	8.2	**Making the Breakthrough in Generalizing Analog Layout Automation: Using Graph CNNs to Identify Circuit Hierarchies** Kunal Kishor*, Meghna Madhusudan*, Jitesh Poojary*, Wenbin Xu+, Steven Burns±, Jiang Hu+, Ramesh Harjani* and Sachin Sapatnekar* *University of Minnesota, +Texas A&M University, ±Intel
17:10 - 17:30	8.3	**Detecting Critical Paths from an STA Graph using Graph-Based Machine Learning Model** Guannan Guo, Tsung-Wei Huang and Martin Wong University of Illinois at Urbana-Champaign
17:30 - 17:50	8.4	**Machine Learning in Analog and RF Circuit Design** Paul Franzon North Carolina State University
17:50 - 18:00		**Discussion and Q&A**
18:30 - 20:30		**Dinner**